REMARKS

By this Amendment, Applicant has amended informalities noted in the specification. Claims 1-10 are pending in the application. In view of the following remarks provided herein, favorable reconsideration in this application is respectfully requested.

The Examiner rejected claims 1-3, 7 and 10 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,326,696 to Horton et al. ("Horton"), and under 35 U.S.C. 103(a) rejected claim 4 as being unpatentable over Horton, claim 5 as being unpatentable over Horton in view of U.S. Patent No. 6,265,771 to Ference et al. ("Ference"), and claims 6, 8 and 9 as being unpatentable over Horton in view of U.S. Patent No. 6,326,696 to Chan et al. ("Chan").

As set forth in claim 1, the present invention is directed to a stack chip module in which a first semiconductor chip, adhered in the groove of a substrate, has a plurality of center pads and a plurality of edge pads. A second semiconductor chip, also having a plurality of center pads which are brought into alignment with the center pads of the first chip, is joined and electrically connected to the first semiconductor chip by a plurality of bumps, interposed between the respective center pads of the two chips.

Horton discloses the use of solder bumps 26 to electrically connect first and second semiconductor chips 16, 18 (column 3, lines 24-27). But there is no teaching or disclosure of center and/or edge pads on the chips 16, 18. That Horton teaches only one connecting element in the connection between the chips is substantiated by the Examiner's need to rely on single element 26 as disclosing both the solder bumps 26 and the pads 26. But this unfairly and improperly eliminates the import of the pads as being a separate feature, a

separateness which is clearly claimed by the present invention. Nor can it be stated that Horton suggests such pads, in that when pads are contemplated, Horton demonstrates through its own text that clear reference will be made to such pads, as evidenced by pads 19 appearing on the bottom surface of the substrate 17. Had Horton envisioned pads on the semiconductor chips 16, 18, surely this would have been set forth in the disclosure thereof in a like manner. But no reference being made thereto, it can only be said that pads on the chips were not contemplated by, nor are they suggested in, Horton.

Nor does the prior art of Ference or Chan teach or suggest center and edge pads within the semiconductor chips. Furthermore, the prior art does not teach or suggest the combined and complementary use of the center pads with the bumps for electrical connection of the chips, disclosing at most one of these features, but not both used together. In fact, that bonding pads and bumps may be used independently effectively teaches against using both at the same time as that could appear to be a needless duplication of function. In addition, the need to align the center pads introduces a further manufacturing requirement not present when bumps alone are used to join the chips at any given point. However, according to the present invention, the combination of center pads and bumps was found to be very effective in producing a stack chip module with good electrical properties, and therefore represents a patentable distinction over the prior art. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claim 1.

For the reasons set forth herein, claim 1 is in condition for allowance. Claims 2-10 are also in condition for allowance as claims properly dependent on an allowable base claim and for the subject matter set forth therein.

Attached hereto is a marked-up version of the changes made to the application by the current amendment. The attached pages are captioned "Version with Markings to Show Changes Made".

Should the Examiner have any questions or comments, the Examiner is cordially invited to telephone the undersigned attorney so that the present application can receive an early Notice of Allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

On page 2, please amend the third full paragraph beginning on line 11, as follows:

--Fig. 1 is a cross sectional view showing a conventional stack package according to a first method. As shown in Fig. 1, two semiconductor packages 10a, 10b are arranged in a stacked arrangement wherein an outer lead of the top package 10a is bonded to that of the bottom package 10b. In the packages 10a, 10b, lead frames 4a, 4b are adhered on one side of each semiconductor chip 1a, 1b by adhesives 3a, 3b, all respectively. Inner leads of each lead frame 4a, 4b are electrically connected to bonding pads 2a, 2b of each semiconductor chip 1a, 1b by gold wires 5a, 5b and the space including each semiconductor chip 1a, 1b and inner leads of lead frames 4a, 4b wire [boned] bonded thereto is molded by molding materials 6a, 6b so that only outer leads of lead frames 4a, 4b are exposed to both sides.--

On page 13, please amend the second full paragraph beginning on line 8, as follows:

--Fig. 9 is a cross sectional view showing a stack chip module according to a fourth embodiment of the present invention. Referring to Fig. 9, grooves T for installing a bottom chip 20 are formed in a jig-jag form, alternating on one side and then on the other side of substrate 30 and therefore, chips 20, 22 are mounted on [oppostie] opposite sides of the substrate 30. Accordingly, it is possible to mount a large number of chips on both sides of the substrate 30, thereby improving the capacity of the module.--